REMARKS

In response to the Office Action mailed April 9, 2004, Applicant respectfully requests reconsideration.

The Office Action suggested a preferred arrangement of the specification. Applicant has amended the specification to include appropriate titles and believes that the arrangement of the specification is appropriate.

The Office Action stated that the title of the invention is not descriptive. Applicant has changed the title to METHOD AND APPARATUS FOR CHECKING AN INCOMING BIT STREAM FOR ERRORS and believes that the title is now clearly indicative of the invention to which the claims are directed. Review and approval of the new title is respectfully requested.

Claims 9, 10, and 11 were objected to under 37 C.F.R. §1.75(c) as being in improper form. Applicant has amended claim 9 to depend from claim 1, claim 10 to depend from claim 1, and claim 11 to depend from claim 3. Accordingly, Applicant believes that the claims now comply with 37 C.F.R. §1.75(c) and respectfully requests withdrawal of the objection.

Claims 1-3 and 12 were rejected under 35 U.S.C. §102(b) as being anticipated by Higuchi et al. In addition, claims 4-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi in view of Erickson et al. Applicant respectfully traverses these rejections.

Figures 1 and 2 of Higuchi show a selector element 40 for selecting which of the flip flops of the CRC generating part are to be used as a final stage from which the output is to be taken, and it is this selected output which is said to be added to the rear of the input data (abstract). Thus, in Higuchi, only a single feedback signal was applied to the data input and only a single feedback signal is output from the selector 40 to the data input 11A of the CRC generating part 10.

By contrast, claim 1 recites, *inter alia*, "a register having a plurality of data input nodes each data input node being selectable to receive data from the data input stage and a set of output feedback nodes arranged to selectively supply a feedback signal to the data input stage". Clearly, Higuchi does not teach or suggest at least a plurality of input feedback nodes as recited in claim 1.

Additionally, Higuchi discloses a number of flip flops each being hardwired to receive data from the data input stage (i.e., the output of element 11A shown as being directly connected

to each of the flip flops in Figure 1 of Higuchi). By contrast, claim 1 recites "a register having a plurality of data input nodes each data input node being selectable to receive data ...". This distinction is further reinforced by the recitation in claim 1 of "multiplexing circuitry... to selectively connect said data node to at least some of said data input nodes". In Higuchi, by contrast, the hardwired or fixed arrangement connects the data from the data node directly to each flip flop via an XOR gate 11. Thus, present claim 1 is distinguished from Higuchi because multiplexing circuitry is provided that allows selectively connecting the data node to at least some of the data input nodes. Higuchi is incapable of selectively connecting said data node to at least some of said data input nodes as recited in claim 1.

Claims 2-11 depend from claim 1 and are allowable for at least the same reasons.

Claim 12 recites a method of checking an incoming bit stream for errors, comprising the steps of receiving at an input stage an incoming bit stream; supplying a plurality of input signals from said input stage to a register arranged to receive the plurality of input signals at a plurality of data input nodes, each data input node being selectable to receive said plurality of input signals, and to generate a plurality of feedback signals; connecting one of said feedback signals to the input stage to perform an error check based on a first mathematical function; and subsequently disconnecting said feedback signal and connecting another one of said feedback signals to the input stage thereby to perform an error check based on a second, different, mathematical function.

As discussed above in connection with claim 1, Higuchi does not teach or suggest at least "supplying a plurality of input signals...connecting one of said feedback signals to the input stage to perform an error check based on a first mathematical function, and subsequently disconnecting the feedback signal and connecting another one of the feedback signals to the input stage..." as recited in claim 12.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the undersigned at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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